

Ex parte Lee et al.

Lee

THIS OPINION WAS NOT WRITTEN FOR PUBLICATION

The opinion in support of the decision being entered today (1) was not written for publication in a law journal and (2) is not binding precedent of the Board.

Paper No. 28

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte JUN HO LEE
and SEONG JAE CHO

Appeal No. 96-1070
Application 07/937,751¹

HEARD: APRIL 9, 1997

MAILED

APR 30 1997

PAT.&T.M. OFFICE
BOARD OF PATENT APPEALS
AND INTERFERENCES

Before HAIRSTON, FLEMING and LEE, *Administrative Patent Judges*.

FLEMING, *Administrative Patent Judge*.

DECISION ON APPEAL

This is a decision on appeal from the final rejection of claims 4 through 21, all of the claims pending in the present application. Claims 1 through 3 have been canceled.

The invention relates to a system for controlling various circuits by utilizing a control bus. In particular, Appellants

¹ Application for patent filed September 1, 1992.

disclose on pages 4 through 6 of the specification and illustrate in Figure 3 that an address is routed to one (e.g. circuit A) of a plurality of circuits A, B and C by enabling a block of AND gates (e.g. AND1-4) that correspond to the one circuit (e.g. circuit A) by a common control line for that block of AND gates connected to each gate input (e.g. line A7) that will allow the address to pass through to the one circuit (e.g. circuit A).

The independent claim 4 is reproduced as follows:

4. An address decoding circuit, comprising:

address latch means for generating first, second, third, fourth, fifth, sixth and seventh latching signals for designating selected ones of a plurality of circuits and corresponding addresses of the selected ones of said plurality circuits to be controlled;

a first group of logic gates, responsive to said first, second, third, fourth and seventh latching signals, for generating first, second, third and fourth addresses representative of addresses of a first one of said plurality of circuits;

a second group of logic gates, responsive to said first, second, third, fourth and sixth latching signals, for generating fifth, sixth, seventh and eighth addresses representative of addresses of a second one of said plurality of circuits; and

a third group of logic gates, responsive to said first, second, third, fourth and fifth latching signals, for generating ninth, tenth, eleventh and twelfth addresses representative of addresses of a third one of said plurality of circuits.

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The Examiner relies on the following references:

Kinghorn et al (Kinghorn)	4,570,154	Feb. 11, 1986
Nozaki	4,716,410	Dec. 29, 1987

"Design Engineer" 1981 Supplement to the TTL Data Book, Texas Instruments Incorporated, Second Edition, pp. 19-22, (June 1978) (hereinafter Texas Instruments I).

"Design Engineers" 1981 Supplement to the TTL Data Book, Texas Instruments Incorporated, Second Edition, pp. 7-181-7-183, (October 1976) (hereinafter Texas Instruments II)

"Advanced Synchronous Data Link Control", IBM Technical Disclosure Bulletin, Vol. 32, No. 11, pp. 116-118, (April 1990) (hereinafter IBM).

Claims 4 through 14 stand rejected under 35 U.S.C. § 103 as being unpatentable over Kinghorn and Texas Instruments I. Claims 15 through 21 stand rejected under 35 U.S.C. § 103 as being unpatentable over Kinghorn, Texas Instruments II, Nozaki and IBM.

Rather than reiterate the arguments of Appellants and the Examiner, reference is made to the briefs² and answer for the respective details thereof.

² Appellants filed an appeal brief on February 22, 1995. We will refer to this appeal brief as simply the brief. Appellants filed a reply appeal brief on July 24, 1995. We will refer to this reply appeal brief as the reply brief. The Examiner stated in the Examiner's letter dated September 18, 1995 that the reply brief has been entered and considered but no further response by the Examiner is deemed necessary.

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OPINION

We will not sustain the rejection of claims 4 through 21 under 35 U.S.C. § 103.

The Examiner has failed to set forth a *prima facie* case. It is the burden of the Examiner to establish why one having ordinary skill in the art would have been led to the claimed invention by the express teachings or suggestions found in the prior art, or by implications contained in such teachings or suggestions. *In re Sernaker*, 702 F.2d 989, 995, 217 USPQ 1, 6 (Fed. Cir. 1983). "Additionally, when determining obviousness, the claimed invention should be considered as a whole; there is no legally recognizable 'heart' of the invention." *Para-Ordnance Mfg. v. SGS Importers Int'l, Inc.*, 73 F.3d 1085, 1087, 37 USPQ2d 1237, 1239 (Fed. Cir. 1995), *citing W. L. Gore & Assocs., Inc. v. Garlock, Inc.*, 721 F.2d 1540, 1548, 220 USPQ 303, 309 (Fed. Cir. 1983), *cert. denied*, 469 U.S. 851 (1984).

In regard to the rejection of claims 4 through 14 under 35 U.S.C. § 103 as being unpatentable over Kinghorn and Texas Instruments I, Appellants argue on pages 4 through 12 of the brief that Kinghorn and Texas Instruments I, together or individually, fail to teach or suggest an address decoding

circuit having an address latch means for generating common latching signals that are provided to each of a plurality of _____ groups of logic gates and each group then producing a distinct output of addresses as recited in Appellants' claims. We note that Appellants' claim 4 recites an "address decoding circuit, comprising: address latch means for generating *first, second, third, fourth*, fifth, sixth and seventh latching signals ... a first group of logic gates, responsive to said *first, second, third, fourth* and seventh latching signals, for generating first, second, third and fourth addresses representative of addresses of a first one of said plurality of circuits; a second group of logic gates, responsive to said *first, second, third, fourth* and sixth latching signals, for generating fifth, sixth, seventh and eighth addresses representative of addresses of a second one of said plurality of circuits; and a third group of logic gates, responsive to said *first, second, third, fourth* and fifth latching signals, for generating ninth, tenth, eleventh and twelfth addresses representative of addresses of a third one of said plurality of circuits." Emphasis added.

The Examiner argues on pages 9 and 10 of the answer that Kinghorn and Texas Instruments I would have suggested to those skilled in the art to modify Kinghorn to obtain Appellants'

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invention as recited in claims 4 through 14. The Examiner states on page 9 of the answer that Kinghorn "illustrates that latched logic single lines 939 may be utilized to select which of three groups 930, 931, 932 of logic gates is to be activated." The Examiner states that Texas Instruments I teaches at page 22 "that a group of logic lines X0-X2 may be utilized to select which of three output devices a common set of logic inputs X3-X5 is to be directed." The Examiner further states on page 10 of the answer that "[s]ince the artisan would have been aware of the need for switch directed data in communications systems which were abundant in the art, the artisan possessing only a routine level of skill in the art would have clearly recognized that the knowledge present only in the prior art provided all that was necessary to suggest to and motivate the artisan to combine the collective teachings of the references to result in the claimed invention."

Appellants point out on page 8 that by incorporating the 'common set of input latching signals' of Texas Instruments I into the Kinghorn circuit, the intended mode of operation of Kinghorn is destroyed because only six of the fourteen key switches on keyswitch 900 are operable. Appellants argue that one of ordinary skill in the art would have no motivation or

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incentive to make the Examiner's proposed modification because the use of common latching signals as taught by Texas Instruments I in Kinghorn results in a circuit that does not fulfill the intended mode of operation of Kinghorn.

The Federal Circuit states that "[t]he mere fact that the prior art may be modified in the manner suggested by the Examiner does not make the modification obvious unless the prior art suggested the desirability of the modification." *In re Fritch*, 972 F.2d 1260, 1266 n.14, 23 USPQ2d 1780, 1783-84 n.14 (Fed. Cir. 1992), *citing In re Gordon*, 733 F.2d 900, 902, 221 USPQ 1125, 1127 (Fed. Cir. 1984). "Obviousness may not be established using hindsight or in view of the teachings or suggestions of the inventor." *Para-Ordnance Mfg. v. SGS Importers Int'l*, 73 F.3d at 1087, 37 USPQ2d at 1239, *citing W. L. Gore & Assocs., Inc. v. Garlock, Inc.*, 721 F.2d at 1551, 1553, 220 USPQ at 311, 312-13. Upon reviewing Kinghorn and Texas Instruments I, we fail to find any suggested desirability of modifying Kinghorn with Texas Instruments I to obtain an address decoding circuit as recited in Appellants' claims 4 through 14.

We note that Kinghorn discloses in column 4, lines 20 through 21 that Figure 5 is a circuit diagram of a data entry keyboard apparatus. In column 11, line 3, through column 12,

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line 60, Kinghorn teaches that the data entry keyboard apparatus shown in Figure 5 enables a key-switch array to comprise a further $2n$ key switches in addition to $n/2 \times (n-1)$ key switches which the array normally comprises for n connection terminals. We agree with the Examiner that Kinghorn teaches a first, second and third group of AND gates 930, 931 and 932 shown in Figure 5. However, Kinghorn's Figure 5 shows that each group of AND gates 930, 931 and 932 has an input from unique signal lines 914, 926 and 929, respectively. Thus, Kinghorn fails to teach an address latch means for generating first, second, third and fourth latching signals and first, second and third groups of logic gates responsive to the first, second, third and fourth latching signals as recited in Appellants' claims 4 through 14.

Texas Instruments I teaches in the Figure on page 22 a six line to sixty-four line decoder. The Figure shows common signals lines X3, X4, X5 provided to each of the three bottom LS137 decoders. The figure also shows another LS137 decoder providing an enabling signal to each of the three bottom LS137 decoders.

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We fail to find any suggestion in either reference to modify Kinghorn by modifying the Kinghorn unique signal lines 914, 926 and 929 to each group of AND gates 930, 931 and 932 with the Texas Instruments I common signals lines. Other than using the Appellants' claims as a road map, we find that the prior art has not suggested such a modification.

In regard to the rejection of claims 15 through 21 under 35 U.S.C. § 103 as being unpatentable over Kinghorn, Texas Instruments II, Nozaki and IBM, we fail to find that the Examiner has shown that these references suggest modifying Kinghorn's unique signal lines 914, 926 and 929 by providing common signals lines to each group of Kinghorn's AND gates 930, 931 and 932 to obtain Appellants' claimed invention. Since there is no evidence in the record that the prior art suggested the desirability of such a modification, we will not sustain the Examiner's rejection of claims 15 and 21.

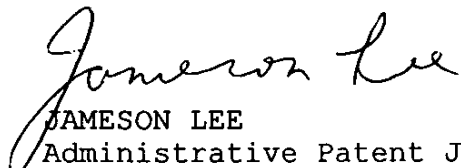
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We have not sustained the rejection of claims 3 through 21
under 35 U.S.C. § 103. Accordingly, the Examiner's decision is
reversed.

REVERSED


KENNETH W. HAIRSTON
Administrative Patent Judge


MICHAEL R. FLEMING
Administrative Patent Judge


JAMESON LEE
Administrative Patent Judge

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